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miss + (FIFO or queue) + pipeline + latency Search

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Lowercase **"or"** was ignored. Try **"OR"** to search for either of two terms. [details]

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All Results

'J Dean
J Hicks
W Weihl
C Waldspurger
G Chrysos

Scaling the issue window with look-ahead **latency** prediction - all 2 versions »
Y Liu, A Shayesteh, G Memik, G Reinman - Proceedings of the 18th annual international conference on ..., 2004 - portal.acm.org
... window that are consumers of an outstanding load **miss**. ... sorting structure with a number of **FIFO** queues to enable instructions to enter the issue **queue** out-of ...
Cited by 13 - Related Articles - Web Search

An effective pixel rasterization **pipeline** architecture for 3D rendering processors - all 7 versions »
WC Park, KW Lee, IS Kim, TD Han, SB Yang - Computers, IEEE Transactions on, 2003 - ieeexplore.ieee.org
... If a tag comparison reveals a **miss**, the cache tag ... The request **FIFO queue** sends a request for the missing cache ... its result is a hit, the **pipeline** execution can ...
Cited by 7 - Related Articles - Web Search - BL Direct

Method for estimating statistics of properties of instructions processed by a processor **pipeline** - all 5 versions »
GZ Chrysos, J Dean, JE Hicks, CA Waldspurger, WE ... - US Patent 5,809,450, 1998 - Google Patents
... US005809450A [ii] Patent Number: [45] Date of Patent: [54] METHOD FOR ESTIMATING STATISTICS OF PROPERTIES OF INSTRUCTIONS PROCESSED BY A PROCESSOR **PIPELINE** ...
Cited by 53 - Related Articles - Web Search

Context switching system for a multi-thread execution **pipeline** loop and method of operation thereof
VA Bennett, SW McGee - 2003 - freepatentsonline.com
... The **queue** engine 316 is coupled to an external control memory 360 and ... a **miss** fulfillment first-in-first-out buffer ("**miss** fulfillment **FIFO**") 550 to ...
Cached - Web Search

Reducing the Energy of Speculative Instruction Schedulers - all 4 versions »
Y Liu, G Memik, G Reinman - Proceedings of the 2005 International Conference on Computer ..., 2005 - doi.ieeecomputersociety.org
... they are buffered in low-power **FIFO** structures ... 16] propose to predict load/hit **miss** information during ... speculative scheduler and the energy of the issue **queue**. ...
Related Articles - Web Search

Processor-Memory Co-Exploration driven by a Memory-Aware Architecture Description Language - all 8 versions »
P Mishra, P Grun, N Dutt, A Nicolau - International Conference on VLSI Design, 2001 - doi.ieeecomputersociety.org
... (**PIPELINE** COL_DEC ROW_DEC PRECHARGE) ... ... When the stream buffer receives an L1 cache **miss** address, it compares it to the top of each **FIFO queue**. ...
Cited by 29 - Related Articles - Web Search

A mid-texturing pixel rasterization **pipeline** architecture for 3D rendering processors - all 6 versions »
TOC View - Application-Specific Systems, Architectures and Processors, ..., 2002 - ieeexplore.ieee.org
... Request **FIFO Queue** ... case can be calculated by multiplying the pixel cache **miss** rate by ... be assumed that one pixel is generated per cycle with one pixel **pipeline**. ...
Cited by 2 - Related Articles - Web Search

Processor Power Reduction Via Single-ISA Heterogeneous Multi-Core Architectures - all 15 versions »
R Kumar, K Farkas, NP Jouppi, P Ranganathan, DM ... - ieeexplore.ieee.org
... of most instructions independent of an L2 **miss** are correctly ... results and INV status into a **FIFO** reuse **queue** ... encounters an INV instruction in the **queue**, it is ...
Cited by 17 - Related Articles - Web Search

Recovery mechanism for **latency** misprediction - all 10 versions »
E Morancho, JM Llaberia, A Olive - Parallel Architectures and Compilation Techniques, 2001. ..., 2001 - ieeexplore.ieee.org
... Figure 1 : **Pipeline** designs without **latency** prediction. Stages: read registers (R), issue **queue** (IQ), compute address (@), execute (exe), data-array access (m ...
Cited by 34 - Related Articles - Web Search

Apparatus for sampling instruction operand or result values in a processor **pipeline** - all 2 versions »
GZ Chrysos, J Dean, JE Hicks, CA Waldspurger, WE ... - US Patent 5,923,872, 1999 - Google Patents
... [54] APPARATUS FOR SAMPLING INSTRUCTION OPERAND OR RESULT VALUES IN A PROCESSOR **PIPELINE** ... Instructions are fetched into a first stage of the **pipeline**. ...

Lowercase "**or**" was ignored. Try "**OR**" to search for either of two terms. [details]

Scholar **All articles** - Recent articles Results **1** - **10** of about **139** for **miss** + **fulfillment** + (**cache** or **buffer** or **queue** or **FIFO**) + **pipeline** + **latency**. (**0.13** seconds)

All Results
K Gharachorloo
T Chen
E Tam
E Rotenberg
J Dundas

Context switching system for a multi-thread execution **pipeline** loop and method of operation thereof
VA Bennett, SW McGee - 2003 - freepatentsonline.com
... DRAM 534, due to a **cache miss** status. ... **fulfillment** first-in-first-out **buffer** ("**miss fulfillment FIFO**") 550 to ... the thread through the **miss fulfillment FIFO** at a ...
Cached - Web Search

[PS] **LATENCY** TOLERANT ARCHITECTURES - all 5 versions »
JE Bennett - 1998 - citeseer.csail.mit.edu
... in partial **fulfillment** of the requirements ... which is large enough to produce a low **miss** rate. ... in his thesis[McF97], the on-chip **cache** size will be limited to 32 ...
Cited by 3 - Related Articles - View as HTML - Web Search - Library Search

The Header-Trailer Trace **Cache**: Efficiently Storing Multipath Traces
GA Rasche - 2004 - crhc.uiuc.edu
... Submitted in partial **fulfillment** of the requirements for the degree of ... have been developed to address the trace **cache miss** problem ...: 3.4.Trace **Cache** Filter **Buffer** ...
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Masking Memory Access **Latency** with a Compiler-Assisted Data Prefetch Controller - all 4 versions »
SP VanderWiel - 1998 - arctic.umn.edu
... IN PARTIAL **FULFILLMENT** OF THE REQUIREMENTS ... Rather than waiting for a **cache miss** to perform a ... **latency** but must be held in the processor **cache** for some period of ...
Related Articles - View as HTML - Web Search - Library Search

Hardware Performance Monitoring in Memory of NUMAchine Multiprocessor - all 4 versions »
EA Pin - 1997 - eecg.toronto.edu
... A THESIS SUBMITTED IN PARTIAL **FULFILLMENT** OF THE REQUIREMENTS FOR THE ... the counters in SPARCcenter 2000 provide data on raw **cache miss** rates and ... secondary **cache** ...
Related Articles - View as HTML - Web Search

Characterizing Logical Masking of Transient Faults at the Microarchitectural and Architectural ... - all 2 versions »
NJ Wang - 2003 - crhc.uiuc.edu
... Submitted in partial **fulfillment** of the requirements for the degree of Master of Science in ... of fault injections into dead state in the L1 data **cache's miss** ...
Related Articles - View as HTML - Web Search - Library Search

DESIGN AND IMPLEMENTATION OF A MULTITHREADED, WIDE WORD OPERATION, PROCESSING IN MEMORY ARCHITECTURE
EKH Kang - 2003 - etd.nd.edu
... in Partial **Fulfillment** of the Requirements ... Width of instruction **cache** 128 1 ... **miss** penalties paid by devices that use speculative execution along with large ...
Cited by 1 - Related Articles - View as HTML - Web Search - Library Search

EXCLUSIVE **CACHE** ARCHITECTURE AND PERFORMANCE EVALUATION - all 3 versions »
Y ZHENG - 2003 - ece.mtu.edu
... hereby approved in partial **fulfillment** of the requirements for the degree of ... **buffer** is full and there is an L1 **miss**/L2 hit. ... same manner as the victim **cache** does ...
Cited by 1 - Related Articles - View as HTML - Web Search - Library Search

MEMORY CONSISTENCY MODELS FOR SHARED-MEMORY MULTIPROCESSORS - all 7 versions »
K Gharachorloo - 1995 - research.compaq.com
... STUDIES OF STANFORD UNIVERSITY IN PARTIAL **FULFILLMENT** OF THE ... these optimizations complement gains from other **latency** hiding techniques ... 132 5.1 **Cache** Coherence ...
Cited by 68 - Related Articles - View as HTML - Web Search - Library Search

[PS] Data Prefetching for High-Performance Processors - all 5 versions »
TF Chen - 1993 - twins.pmf.ukim.edu.mk
... In presenting this dissertation in partial **fulfillment** of the ... on a **cache miss**, where those b-byte blocks are ... data be in the **cache** "just in time" to ...
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All Results

E Rotenberg
T Chen
D Chaiken
K Sundaramoort...
M Fillo

Loose loops sink chips - all 13 versions »
E Borch, E Tune, S Manne, J Emer - ieeexplore.ieee.org
... The forwarding **buffer** is required for the base architecture ... for 100 million instructions total for both **threads**. ... has a reasonably high data **cache miss** rate; how ...
Cited by 106 - Related Articles - Web Search

A scalable instruction **queue** design using dependence chains - all 13 versions »
SE Raasch, NL Binkert, SK Reinhardt - Computer Architecture, 2002. Proceedings. 29th Annual ..., 2002 - ieeexplore.ieee.org
... the same as the "issue **buffer**" discussed above ... Each instruction **queue** entry maintains four fields for ... predicted **latency**—eg, when a **cache miss** is detected ...
Cited by 55 - Related Articles - Web Search - BL Direct

Pointer **cache** assisted prefetching - all 17 versions »
J Collins, S Sair, B Calder, DM Tullsen - Microarchitecture, 2002.(MICRO-35). Proceedings. 35th Annual ..., 2002 - ieeexplore.ieee.org
... time) 2048KB, 8-way shared L3 **cache** (30 cycle ... handled by pipelined, on chip TLB **miss** handler, 60 ... access time Multithreading 8 total hardware **thread** contexts ...
Cited by 50 - Related Articles - Web Search - BL Direct

Slipstream processors: improving both performance and fault tolerance - all 18 versions »
K Sundaramoorthy, Z Purser, E Rotenberg - ACM SIGPLAN Notices, 2000 - portal.acm.org
... in the A-stream and communicating state between the **threads**. ... a 64-entry ROB (a shared level-two **cache** always hits ... The **delay buffer length** is 256 instruc- tions. ...
Cited by 137 - Related Articles - Web Search - BL Direct

Reducing memory **latency** via non-blocking and prefetching caches - all 9 versions »
TF Chen, JL Baer - ACM SIGPLAN Notices, 1992 - portal.acm.org
... switching can hide the memory **latency** of a **thread** or of ... cycle is required to modify the data block in the **cache**. ... due to write **miss** has priority over prefetches ...
Cited by 178 - Related Articles - Web Search - Library Search - BL Direct

Context switching system for a multi-**thread** execution **pipeline** loop and method of operation thereof
VA Bennett, SW McGee - 2003 - freepatentsonline.com
... the DRAM 534, due to a **cache miss** status. ... system 520 advantageously employs the **miss** fulfillment **FIFO** ... to start executing in the multi-**thread** execution **pipeline** ...
Cached - Web Search

SMTp: an architecture for next-generation scalable multi-threading - all 12 versions »
M Chaudhuri, M Heinrich - Computer Architecture, 2004. Proceedings. 31st Annual ..., 2004 - ieeexplore.ieee.org
... Whenever a protocol **thread** load/store **miss** conflicts with ... The L1 and L2 **cache** controllers are augmented with ... First, the short proto- col **thread** handlers suffer ...
Cited by 5 - Related Articles - Web Search - BL Direct

Method for estimating statistics of properties of instructions processed by a processor **pipeline** - all 5 versions »
GZ Chrysos, J Dean, JE Hicks, CA Waldspurger, WE ... - US Patent 5,809,450, 1998 - Google Patents
... Compi -lation Using the Profile **Buffer**, Proceedings of ... selected instruction are processed by the **pipeline**. ... Page Mapping Policies for **Cache** Conflict Resolution ...
Cited by 53 - Related Articles - Web Search

Reducing the complexity of the issue logic - all 17 versions »
R Canal, A González - Proceedings of the 15th international conference on ..., 2001 - portal.acm.org
... lines, 1- cycle hit time, 6-cycle **miss** penalty 3 ... I/D-**cache** L2 256 KB, 4-way set associative ... suffers significant performance degradation when the I-**buffer** is not ...
Cited by 41 - Related Articles - Web Search

Continual flow pipelines - all 2 versions »
ST Srinivasan, R Rajwar, H Akkary, A Gandhi, M ... - ACM SIGARCH Computer Architecture News, 2004 - portal.acm.org
... throughput while still achieving high single **thread** performance compared ... On an L2 **cache** load **miss**, the NAV ... **Cache** and Functional units L2 **Cache** Memory Interface ...
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thread + miss + (cache or buffer or (Search

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All Results

T Chen
E Tam
K Gharachorloo
E Rotenberg
G Semeraro

Context switching system for a multi-thread execution **pipeline** loop and method of operation thereof
VA Bennett, SW McGee - 2003 - freepatentsonline.com
... DRAM 534, due to a **cache miss** status. ... **fulfillment** first-in-first-out **buffer** ("**miss fulfillment FIFO**") 550 to ... the thread through the **miss fulfillment FIFO** at a ...
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[PS] LATENCY TOLERANT ARCHITECTURES - all 5 versions »
JE Bennett - 1998 - citeseer.csail.mit.edu
... in partial **fulfillment** of the requirements ... which is large enough to produce a low **miss** rate. ... in his thesis[McF97], the on-chip **cache** size will be limited to 32 ...
Cited by 3 - Related Articles - View as HTML - Web Search - Library Search

The Header-Trailer Trace **Cache**: Efficiently Storing Multipath Traces
GA Rasche - 2004 - crhc.uiuc.edu
... Submitted in partial **fulfillment** of the requirements for the degree ... it is still in the filter **buffer** exceeds a ... a fetch results in a trace **cache miss**, a trace ...
Related Articles - View as HTML - Web Search - Library Search

Multiple Clock Domain Microarchitecture Design and Analysis
GP Semeraro - 2003 - ce.rit.edu
... A Thesis Submitted in Partial **Fulfillment** of the ... capable of executing other instructions when the **cache miss** occurs ... the instruction **cache** with a trace **cache** [93 ...
Cited by 6 - Related Articles - Web Search - Library Search

Masking Memory Access **Latency** with a Compiler-Assisted Data Prefetch Controller - all 4 versions »
SP VanderWiel - 1998 - arctic.umn.edu
... IN PARTIAL **FULFILLMENT** OF THE REQUIREMENTS ... in Figure 4d, let us assume an average **miss latency** of 100 ... That is, as the **cache** block size increases, so does the ...
Related Articles - View as HTML - Web Search - Library Search

Slipstream Processors
ZR Purser - 2003 - lib.ncsu.edu
... in partial **fulfillment** of the ... leading to mispredicted branches and loads that **miss** in the level ... proposed run-ahead to improve first-level data **cache** performance ...
Cited by 3 - Related Articles - View as HTML - Web Search - Library Search

EXCLUSIVE **CACHE** ARCHITECTURE AND PERFORMANCE EVALUATION - all 3 versions »
Y ZHENG - 2003 - ece.mtu.edu
... hereby approved in partial **fulfillment** of the requirements for the degree of ... **buffer** is full and there is an L1 **miss**/L2 hit. ... same manner as the victim **cache** does ...
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DESIGN AND IMPLEMENTATION OF A MULTITHREADED, WIDE WORD OPERATION, PROCESSING IN MEMORY ARCHITECTURE
EKH Kang - 2003 - etd.nd.edu
... in Partial **Fulfillment** of the Requirements ... Width of instruction **cache** 128 1 ... **miss** penalties paid by devices that use speculative execution along with large ...
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[PS] Data Prefetching for High-Performance Processors - all 5 versions »
TF Chen - 1993 - twins.pmf.ukim.edu.mk
... In presenting this dissertation in partial **fulfillment** of the ... on a **cache miss**, where those b-byte blocks are ... data be in the **cache** "just in time" to ...
Cited by 55 - Related Articles - View as HTML - Web Search - Library Search

ON-CHIP MULTIPROCESSOR COMMUNICATION NETWORK DESIGN AND ANALYSIS - all 3 versions »
TT Ye - 2003 - akebono.stanford.edu
... in partial **fulfillment** of the requirements ... 5.6 **Cache Miss** Penalty under Different Packetization Schemes . ... 87 5.11 **Cache** Energy Decrease as Packet Payload Size ...
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Lowercase "or" was ignored. Try "OR" to search for either of two terms. [details]

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All Results
T Chen
D Chaiken
E Rotenberg
K Sundaramoort...
J Baer

The VMP network adapter board (NAB): high-performance network communication for multiprocessors
H Kanakia, D Cheriton - Applications, Technologies, Architectures, and Protocols for ..., 1988 - portal.acm.org
... for network data transfers, would also increase **cache miss** ratio for ... an RAR, and the availability of **buffer** memory to ... A short **FIFO** is included in the NAC to ...
Cited by 96 - Related Articles - Web Search

History-based prefetch **cache** including a time **queue** - all 2 versions »
AD Berenbaum, TE Jeremiassen... - US Patent 5,778,435, 1998 - Google Patents
... the steps of: a) inserting, when a **cache miss** occurs, amissing ... of the instruction in the prefetch target **buffer** and placing it in the **cache** to prevent ...
Cited by 24 - Related Articles - Web Search

Loose loops sink chips - all 13 versions »
E Borch, E Tune, S Manne, J Emer - ieeexplore.ieee.org
... M instructions out of an instruction **queue** of N ... The forwarding **buffer** is required for the base architecture ... apsi has a reasonably high data **cache miss** rate; how ...
Cited by 106 - Related Articles - Web Search

A scalable instruction **queue** design using dependence chains - all 13 versions »
SE Raasch, NL Binkert, SK Reinhardt - Computer Architecture, 2002. Proceedings. 29th Annual ..., 2002 - ieeexplore.ieee.org
... the same as the "issue **buffer**" discussed above ... Each instruction **queue** entry maintains four fields for ... predicted **latency**—eg, when a **cache miss** is detected ...
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Scaling the issue window with look-ahead **latency** prediction - all 2 versions »
Y Liu, A Shayesteh, G Memik, G Reinman - Proceedings of the 18th annual international conference on ..., 2004 - portal.acm.org
... the issue window that are consumers of an outstanding load **miss**. ... **latency** can range from the L1 **cache** hit **latency** ... The pre-issue **buffer** of this sorting structure ...
Cited by 13 - Related Articles - Web Search

Reducing memory **latency** via non-blocking and prefetching caches - all 9 versions »
TF Chen, JL Baer - ACM SIGPLAN Notices, 1992 - portal.acm.org
... of the total data access penalty, even without a write **buffer**. ... is required to modify the data block in the **cache**. ... due to write **miss** has priority over prefetches ...
Cited by 178 - Related Articles - Web Search - Library Search - BL Direct

Slipstream processors: improving both performance and fault tolerance - all 18 versions »
K Sundaramoorthy, Z Purser, E Rotenberg - ACM SIGPLAN Notices, 2000 - portal.acm.org
... The **delay buffer** is a simple **FIFO queue** that allows the A ... and a 64-entry ROB (a shared level-two **cache** always hits ... The **delay buffer length** is 256 instruc- tions. ...
Cited by 137 - Related Articles - Web Search - BL Direct

Reducing data **cache** energy consumption via cached load/store **queue** - all 8 versions »
D Nicolaescu, A Veidenbaum, A Nicolau - Proceedings of the 2003 international symposium on Low power ..., 2003 - portal.acm.org
... increased load **latency** in the case of a filter **cache miss**, but the ... 512KB 2-way set associative, 12 cycle unified L2 **cache**, and 80 ... The reorder **buffer** size is 64 ...
Cited by 7 - Related Articles - Web Search

High Frequency **Pipeline** Architecture Using the Recirculation **Buffer** - all 4 versions »
M Gschwind, S Kosonocky, E Altman - IBM Research Report (RC23113), 2001 - research.ibm.com
... Recirc **Buffer** Ins **Buffer** ... performance re- gardless stall the machine even if a **cache-miss** value being ... 6. Thus, if such a packet incurs a TLB **miss** (or page fault ...
Cited by 3 - Related Articles - View as HTML - Web Search

Recovery mechanism for **latency** misprediction - all 10 versions »
E Morancho, JM Llaberia, A Olive - Parallel Architectures and Compilation Techniques, 2001. ..., 2001 - ieeexplore.ieee.org
... 5 gives performance results of the recovery-**buffer** mechanism compared ... if data- array .access is a **cache** hit. ... includes a stage between the issue **queue** and the ...
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D Chaiken
T Chen
M Fillo
J Kubiatowicz
A Agarwal

The VMP network adapter board (NAB): high-performance network communication for multiprocessors
H Kanakia, D Cheriton - Applications, Technologies, Architectures, and Protocols for ..., 1988 - portal.acm.org
... In addition, the **context switch** may also incur contention ... data transfers, would also increase **cache miss** ratio for ... and the availability of **buffer** memory to ...
Cited by 96 - Related Articles - Web Search

LimitLESS directories: A scalable **cache** coherence scheme - all 22 versions »
D Chaiken, J Kubiatowicz, A Agarwal - Proceedings of the fourth international conference on ..., 1991 - portal.acm.org
... Unlike a full-map directory, the size of a limited directory ... munication locality, reduces average communication **latency** ... Shared-data **caching** in ...
Cited by 216 - Related Articles - Web Search - Library Search

Context switching system for a multi-thread execution **pipeline** loop and method of operation thereof
VA Bennett, SW McGee - 2003 - freepatentsonline.com
... such as the DRAM 534, due to a **cache miss** status. ... [0059] The **context switching** system 520 ... a **miss** fulfillment first-in-first-out **buffer** ("**miss** fulfillment **FIFO** ...
Cached - Web Search

Cluster **miss** prediction for instruction caches in embedded networking applications
K Batcher, R Walker - Great Lakes Symposium on VLSI, 2004 - portal.acm.org
... a distant sub-routines, or handling a **context switch** in response ... For POM, a **miss** resulted in an average of 49 ... cycles since commonly 1-2 full **cache** lines where ...
Cited by 2 - Related Articles - Web Search

[PS] Ar-smt: Coarse-grain time redundancy for high performance general purpose processors - all 3 versions »
E Rotenberg - Univ. of Wisc. Course Project(ECE753), http://www. cs. wisc. ..., 1998 - tinker.ncsu.edu
... When resuming after a **context switch** (or upon starting ... instruction **cache** size/assoc/repl = 128kB/4-way/LRU ... 16 instructions 2-way interleaved **miss** penalty = ...
Cited by 1 - Related Articles - View as HTML - Web Search

The M-Machine multicomputer - all 15 versions »
M Fillo, SW Keckler, WJ Dally, NP Carter, A Chang, ... - Proceedings of the 28th annual international symposium on ..., 1995 - portal.acm.org
... units, 2 register files, an instruction **cache** and ports onto the memory and cluster **switches**. ... identifiers via a global translation lookaside **buffer** (GTLB ...
Cited by 160 - Related Articles - Web Search - BL Direct

Reducing memory **latency** via non-blocking and prefetching caches - all 9 versions »
TF Chen, JL Baer - ACM SIGPLAN Notices, 1992 - portal.acm.org
... **context-switching** can hide the memory **latency** of a thread or of a ... is required to modify the data block in the **cache**. ... to write **miss** has priority over prefetches ...
Cited by 178 - Related Articles - Web Search - Library Search - BL Direct

Slipstream processors: improving both performance and fault tolerance - all 18 versions »
K Sundaramoorthy, Z Purser, E Rotenberg - ACM SIGPLAN Notices, 2000 - portal.acm.org
... **context** is recovered from the R-stream **context** with relatively ... is indi- cated with an open-**switch** symbol between ... entry ROB (a shared level-two **cache** always hits ...
Cited by 137 - Related Articles - Web Search - BL Direct

SMTp: an architecture for next-generation scalable multi-threading - all 12 versions »
M Chaudhuri, M Heinrich - Computer Architecture, 2004. Proceedings. 31st Annual ..., 2004 - ieeexplore.ieee.org
... the protocol thread to a hardware **context** that does ... Other than **switch** and ldctxt, there are a few ... Whenever a protocol thread load/store **miss** conflicts with an ...
Cited by 5 - Related Articles - Web Search - BL Direct

QSNET/sup II: defining high-performance network design - all 6 versions »
J Beecroft, D Addison, D Hewson, M McLaren, D ... - Micro, IEEE, 2005 - ieeexplore.ieee.org
... a CPU interrupt or an instruction-**cache miss** occurs ... the state of another thread running in another **context**. ... 5 shows the optical interface with a 16- way **switch**. ...
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